AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently Amended) A system embodied on a computer readable storage medium that when executed on one or more processors facilitate processing rules, comprising:

a translator component that translates synchronous statements to asynchronous instructions using a synchronous programming model;

a runtime engine that reads the translated instructions and facilitates efficient scheduling and parallel processing of the translated instructions;

in which the instructions facilitate at least one of yielding to runtime rule code execution switching and calling a utility function, and

in which the translated instructions are scheduled for processing based upon a polling structure, which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

2. (Original) The system of claim 1, the statements are organized into a series of rule types.

3. (Original) The system of claim 2, the rule types express logic that determines the desired state of a target resource.

4. (Original) The system of claim 3, in response to a desired state, and action is taken.

5. (Original) The system of claim 1, the translator component facilitates instantiation of the asynchronous instructions.

6. (Cancelled)

7. (Currently Amended) The system of claim [[6]]1, the instructions facilitate maintaining all states by the runtime engine, which states include at least one of arguments and local variables.

8. (Cancelled)

9. (Original) The system of claim 1, the instructions insert periodic yield statements.

10. (Original) The system of claim 1, the translator component facilitates depth-first traversal to generate at least one of labels and temporary variables for corresponding nodes.

11. (Original) The system of claim 1, the translator component translates modules of the rules into classes.

12. (Currently Amended) The system of claim 1, the instruction includes an address code representation to facilitate context switching by [[a]]the runtime engine.

13. (Original) The system of claim 12, the address code representation employs at least three address codes, which representation is used when a statement or expression includes an asynchronous call.

14. (Original) The system of claim 1, the instructions are translated into a series of instruction blocks that are separated into switch-case blocks.

15. (Original) The system of claim 14, instructions within the instruction block are executed as a unit, and yield to runtime execution only between such instruction blocks.

16. (Original) The system of claim 14, the series of instruction blocks has associated therewith an update identifier that maintains which instruction block of the series is to be executed next upon reentry into the rule.

17. (Currently Amended) A system embodied on a computer readable storage medium that when executed on one or more processors facilitates concurrent processing of rules, comprising:

a translator component that translates the rules into instructions for concurrent processing; and

a runtime engine that schedules the instructions for processing and processes some or all of the instructions concurrently according to the schedule,

the instructions are translated for processing based upon a polling structure, which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

18. (Original) The system of claim 17, the runtime engine facilitates implicit concurrent processing of the rules.

19. (Original) The system of claim 17, the runtime engine receives both the instructions and configuration data, which configuration data specifies at least one of which rules to run and the parameters required to run the rule.

20. (Currently Amended) A system embodied on a computer readable storage medium that when executed on one or more processors facilitates processing rules in a model-based management architecture, comprising:

a plurality of rules that express health criteria for the architecture;

a translator component that translates the rules into asynchronous instructions for concurrent processing; and

a runtime engine that schedules the translated instruction for processing and processes some or all of the instructions concurrently according to the schedule,

wherein the runtime engine schedules execution of an execution stack based on a polling structure for the current frame and the polling structure that is at the top of the execution stack.

21. (Original) The system of claim 20, the runtime engine operates according to one of the instructions that suspends processing of code and waits for an event to occur, in response to which processing of the code is resumed and allowed to act on the event.

22. (Original) The system of claim 20, one of the plurality of rules invokes another rule.

23. (Cancelled)

24. (Original) The system of claim 20, the instruction component includes a language that facilitates looping, such that prior to jumping, a rule returns to the runtime engine to facilitate non-pre-emptive scheduling.

25. (Original) The system of claim 20, the translated instructions facilitate cooperative multitasking so that an execution state of a function is preserved, and constituted at a later time.

26. (Original) The system of claim 20, the instruction facilitate constructing a call frame, which call frame includes at least one of a function parameter, current instruction block, current function, and local variable.

27. (Original) The system of claim 20, the runtime engine includes a spreading algorithm that spreads execution of tasks over a duration of time beginning from an arbitrary time to reduce over-utilization.

28. (Original) A computer system according to the system of claim 20.

29. (Currently Amended) A method of processing rules, comprising:

receiving a plurality of the rules;

translating the rules into instructions for communication to a runtime engine;

scheduling the translated instructions for processing by the runtime engine;

processing at least two of the plurality of instructions concurrently with the runtime engine; ~~and~~

receiving configuration data into the runtime engine to instantiate the rules;

injecting yield instructions into the rule to facilitate yielding execution of the rule to rule code execution switching during processing by the runtime engine, and to facilitate calling utility functions provided by the runtime engine; and .

scheduling the translated instructions for processing based upon a polling structure, which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

30. (Cancelled)

31. (Original) The method of claim 29, the translated instructions are translated into a series of instruction blocks, wherein commencement of execution of the instruction block causes the instruction block to be executed in its entirety before yielding to the runtime engine.

32. (Original) The method of claim 29, further comprising during a startup process, building a task list of rules marked for execution by the runtime engine at startup, and spreading out initiation of the rules in batches such that each batch of rules is scheduled for processing within a time configured time interval.

33. (Original) The method of claim 32, further comprising configuring the time interval based upon predetermined criteria, which criteria includes a number of processors utilized by the computer.

34. (Original) The method of claim 29, the instructions are scheduled for processing in batches by the runtime engine, such that rules of a batch are scheduled for processing uniformly over associated time interval for processing the batch.

35. (Cancelled)

36. (Original) The method of claim 29, scheduling is performed according to a non-preemptive scheduling regime.

37. (Currently Amended) A system embodied on a computer readable storage medium that when executed on one or more processors for processing rules, comprising:

means for receiving a plurality of the rules;

means for converting the rules into instructions;

means for translating the instructions for processing by a runtime engine; ~~and~~

means for scheduling and processing concurrently at least two of the plurality of instructions;

means for injecting yield instructions into the rule to facilitate yielding execution of the rule to rule code execution switching during processing by the runtime engine, and to facilitate calling utility functions provided by the runtime engine; and

means for scheduling the translated instructions for processing based upon a polling structure, which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

38. (Original) The system of claim 37, the means for converting includes means for inserting control relinquishment code into the rule that determines where to relinquish control of the associated translated instruction during execution thereof, which relinquishment code is associated with a stack frame that contains at least one of parameters, local variables, and where in the translated instruction to jump upon reentry.

39. (Original) The system of claim 37, further comprising means for task switching between rules, where the translated instructions includes call frames to facilitate task switching.

40. (Currently Amended) A computer-readable medium having computer-executable instructions for performing concurrent processing of rules, comprising:

a translator component that translates synchronous rule statements into asynchronous instructions using a synchronous programming model;

in which instructions facilitate calling utility functions and yielding to runtime code execution switching of the runtime engine;

wherein the instructions inject yield instructions into the rule to facilitate yielding execution of the rule to rule code execution switching during processing by the runtime engine, and to facilitate calling utility functions provided by the runtime engine and

the instructions are translated for processing based upon a polling structure, which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

41. (New) The system of claim 1, wherein the instructions are scheduled for processing in batches by the runtime engine, such that rules of a batch are scheduled for processing uniformly over associated time interval for processing the batch.

REMARKS

Claims 1-5, 7, 9-20, 21-22 and 24-29, and 31-34, and 36-40 are currently pending in the subject application and are presently under consideration. Claims 1, 17, 20, 29, 37, and 40 have been amended as shown on pp. 2-8 of the Reply. In addition, claims 6, 8, 23, 30, and 35 have been cancelled without prejudice or disclaimer on pages 2-3 and 5-7 of the Reply. Moreover, new claim 41 is hereby presented for consideration with this Reply.

Applicants' representatives thank the Examiner for the courtesies extended during the telephonic interview of July 15, 2008. The Examiner indicated that an updated power of attorney should be filed for this case to include Attorney Matthew Clapper (Reg. 62,216) as an attorney of record in this case. However, the Declaration as originally filed provides power of attorney to registered attorneys and agents associated with customer number 27195, in accordance with MPEP §402 and §403, which customer number includes Matthew Clapper therein. Accordingly, it is respectfully submitted that no new power of attorney should be filed in this case. In addition, at the interview various novel aspects of the claimed subject matter were discussed with respect to deficiencies of the cited art. In particular, it was noted that the prior art does not teach or suggest a runtime engine that schedules based upon a polling structure in which processing occurs for at least one of the polling structure of a current frame and the polling structure at the tops of a stack.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1-28 and 37-39 Under 35 U.S.C. §101

Claims 1-28 and 37-39 stands rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter.

Independent claims 1, 17, 20, and 37 have been amended to overcome any deficiencies related to this rejection. Therefore, dependant claims 2-16, 16-19, 21-28, and 38-39 have overcome any deficiencies related from the since they are dependant from 1,17,20, and 37.

II. Rejection of Claims 1-19, 29-31, 34, 36-40 Under 35 U.S.C. §102(e)

Claims 1-19, 29-31, 34, 36-40 stand rejected under 35 U.S.C. §102(e) as being anticipated by Bigus (2004/0083454). It is respectfully submitted that this rejection should be